

11-13-00

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 62061.0105

First Inventor Cavanaugh

Simulates the Execution of Parallel Instructions in
Title Processor Functional Verification Testing

Express Mail Label No. EF061831262US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. Applicant claims small entity status.
See 37 CFR 1.27.
3. Specification [Total Pages 50]
 - Descriptive title of the invention
 - Cross Reference to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to sequence listing, a table, or a computer program listing appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
4. Drawing(s) (35 U.S.C. 113) [Total Sheets 5]
5. Oath or Declaration [Total Pages 6]
 - a. Newly executed (original or copy)
 - b. Copy from prior application (37 CFR 1.63 (d))
(for continuation/divisional with Box 18 completed)
- i. **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. Application Data Sheet. See 37 CFR 1.76

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

7. CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
 - a. Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. CD-ROM or CD-R (2 copies); or
 - ii. paper
 - c. Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. Assignment Papers (cover sheet & document(s))
10. 37 CFR 3.73(b) Statement Power of
(when there is an assignee) Attorney
11. English Translation Document (if applicable)
12. Information Disclosure Statement (IDS)/PTO-1449 Copies of IDS
Citations
13. Preliminary Amendment
14. Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
15. Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. Request and Certification under 35 U.S.C. 122
(b)(2)(B)(i). Applicant must attach form PTO/SB/35
or its equivalent.
17. Other:

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

 Continuation Divisional Continuation-in-part (CIP)

of prior application No. _____ / _____

Prior application information

Examiner _____

Group Art Unit _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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FEE TRANSMITTAL

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Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT (\$ 725.00)

Complete if Known

Application Number	921-10007
Filing Date	11/10/00
First Named Inventor	Cavanaugh
Examiner Name	
Group Art Unit	
Attorney Docket No.	62061.0105

11/10/00

METHOD OF PAYMENT

1. The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number	11-0851
Deposit Account Name	Booth & Wright, L.L.P.

Charge Any Additional Fee Required
Under 37 CFR 1.16 and 1.17

Applicant claims small entity status.
See 37 CFR 1.27

2. Payment Enclosed:

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
101 710	201 355	Utility filing fee	355.00
106 320	206 160	Design filing fee	
107 490	207 245	Plant filing fee	
108 710	208 355	Reissue filing fee	
114 150	214 75	Provisional filing fee	

SUBTOTAL (1) (\$ 355.00)

2. EXTRA CLAIM FEES

	Extra Claims	Fee from below	Fee Paid
Total Claims	30	-20** = 10	9.00 = 90.00
Independent Claims	10	-3** = 7	40.00 = 280.00
Multiple Dependent			

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description
103 18	203 9	Claims in excess of 20
102 80	202 40	Independent claims in excess of 3
104 270	204 135	Multiple dependent claim, if not paid
109 80	209 40	** Reissue independent claims over original patent
110 18	210 9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$ 370.00)

**or number previously paid, if greater; For Reissues, see above

3. ADDITIONAL FEES

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid
105 130	205 65	Surcharge - late filing fee or oath	
127 50	227 25	Surcharge - late provisional filing fee or cover sheet	
139 130	139 130	Non-English specification	
147 2,520	147 2,520	For filing a request for ex parte reexamination	
112 920*	112 920*	Requesting publication of SIR prior to Examiner action	
113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action	
115 110	215 55	Extension for reply within first month	
116 390	216 195	Extension for reply within second month	
117 890	217 445	Extension for reply within third month	
118 1,390	218 695	Extension for reply within fourth month	
128 1,890	228 945	Extension for reply within fifth month	
119 310	219 155	Notice of Appeal	
120 310	220 155	Filing a brief in support of an appeal	
121 270	221 135	Request for oral hearing	
138 1,510	138 1,510	Petition to institute a public use proceeding	
140 110	240 55	Petition to revive - unavoidable	
141 1,240	241 620	Petition to revive - unintentional	
142 1,240	242 620	Utility issue fee (or reissue)	
143 440	243 220	Design issue fee	
144 600	244 300	Plant issue fee	
122 130	122 130	Petitions to the Commissioner	
123 50	123 50	Petitions related to provisional applications	
126 240	126 240	Submission of Information Disclosure Stmt	
581 40	581 40	Recording each patent assignment per property (times number of properties)	
146 710	246 355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149 710	249 355	For each additional invention to be examined (37 CFR § 1.129(b))	
179 710	279 355	Request for Continued Examination (RCE)	
169 900	169 900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$)

SUBMITTED BY

Complete (if applicable)

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Signature	<i>Karen S. Wright</i>			Date	11/10/2000

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PATENT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

Inventor(s): Cavannaugh et al.
Serial No.:
Filed: New Application
For: Method and Apparatus that Simulates the Execution of Parallel Instructions in
Processor Functional Verification Testing
Docket No.: 62061.0105

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This application claims the benefit of the earlier filed US Provisional Pat. App. Ser. No. 60/165,204, filed 12 November 1999 (12.11.99), entitled "Method and Apparatus for Processor Verification" which is incorporated by reference for all purposes into this specification.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to the functional verification of integrated circuit hardware designs. In particular, the present invention provides a method and apparatus that functionally verifies processors capable of executing more than one instruction at the same architectural time.

Description of the Related Art

Random test generation programs have been around since the early days of microprocessor verification. These programs automate the complex job of creating large test suites necessary for the functional verification of computer systems. From a historic perspective, functional verification has focused on two types of circuits, combinatorial and sequential. Combinatorial circuits do not contain state information, and therefore the outputs are strictly a function of the input values. Sequential circuits contain memory elements that allow the circuit to have a current state. This makes the output values a function of both the current state and the input values. Early on, those in the industry recognized that creating purely random input values was not an adequate method of verifying sequential circuits, and a new test methodology that included the current state of the circuit was developed.

One method used to generate test patterns for processor verification that is well known in

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1 the art is to use a computer to generate a machine executable program that is assembled from
2 instructions, control flags, and data selected from specially prepared tables. To get the expected
3 results, the automatically-assembled test program is simulated on an existing hardware or
4 software golden model under driver control. The test operator can change the drivers, thus
5 changing the conditions under which the test programs are executed. This approach to testing is
6 generally characterized as *static* testing, because the test patterns are assembled first, and are
7 then executed in the simulation to get the expected results. The test pattern development process
8 is not influenced by the intermediate machine states of the processor during the execution of the
9 test.

10 While static testing is highly useful, it does have drawbacks. One obvious drawback is
11 that tests created without knowledge of the intermediate machine states have great difficulty
12 achieving high coverage of all the possible intermediate states. In addition, statically generated
13 tests are restricted in that certain real-life cases can never be simulated. For example, some
14 instructions within a statically generated instruction sequence must always be preceded by a
15 specially-inserted data initialization instruction, which would ordinarily not appear in normal
16 operation. Similarly, register usage can be somewhat more limited in a static simulation than it
17 would ordinarily be in normal operation. Finally, statically generated simulations that include
18 loops and branches must be very carefully (and therefore, artificially) constructed to avoid
19 undesirable test results such as endless loops, branches that are never taken, and the like.

20 To address some of these issues, and to create a test environment that is more efficient
21 and conducts a more robust test of very complex sequential circuits such as processors, the
22 industry has moved toward the use of dynamically generated, biased pseudo-random test

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1 patterns. In dynamic testing, instructions are generated, all processor resources and facilities
2 needed for executing the instruction are identified and initialized if required, the instruction is
3 executed on a simulated processor, and the simulated processor state is updated to reflect the
4 execution results. The process iterates, and each instruction generated at the beginning of each
5 iteration is generated with knowledge of the processor state that resulted from the last step
6 executed. Although there are differences in the details of how instructions are generated from
7 test method to test method, in general, instructions are drawn from an instruction pool or tree
8 specified by the test operator that contains the various types of instructions to be tested. In
9 addition, many pseudo-random dynamic test generation methodologies allow the test operator to
10 bias the instruction pool or tree, meaning that the operator can specify what percentage of the
11 total instructions generated and simulated should be load-store instructions, what percentage
12 should be arithmetic instructions, what percentage should be floating point instructions, and so
13 forth. Those skilled in the art are generally familiar with the various current methods used to
14 conduct functional verification of complex circuits using dynamically generated biased psuedo-
15 random test patterns. Readers unfamiliar with these methods are referred to US Pat. No.
16 5,202,889 to Aharon et al., entitled "Dynamic Process For The Generation Of Biased Pseudo-
17 Random Test Patterns For The Functional Verification Of Hardware Designs" and the patents
18 and publications referenced therein, which is incorporated by reference for all purposes into this
19 disclosure. U.S. Patent No. 5,202,889 to Aharon is a good example of the current state of the art
20 of pseudo-random test pattern generators and their usefulness for functional verification of
21 complex circuits.

22 Dynamic testing conducted in the manner described by Aharon eliminates the

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1 requirement for the cumbersome predevelopment of data tables and code streams that is
2 necessary to achieve a high level of confidence in static testing. Also, because instructions can
3 be automatically and iteratively generated and then simulated using an appropriately biased
4 instruction pool, dynamic testing can also provide greater test coverage than static testing in a
5 shorter amount of time. Nevertheless, dynamically generated tests using psuedo-random test
6 patterns such as that described by Aharon have drawbacks and limitations as well.

7 For example, generating stimuli based solely upon current machine state information may
8 not adequately test some complex processors such as Very Long Instruction Word (“VLIW”)
9 and Reduced Instruction Set Computer (“RISC”) processors, which may have special rules
10 regarding usage of certain resources. Similarly, some processor architectures allow certain
11 groups of instructions to execute at the same architectural time. Instructions that are dynamically
12 generated and simulated in a pseudo-random test pattern must therefore adhere to the processor’s
13 instruction grouping rules. This creates another case where the creation of input stimulus is not
14 just a function of the current state, and therefore requires additional components in the test
15 generator to restrict the grouping of instructions and possible operands to a given set of rules. In
16 addition, while a dynamically generated test setup may run flawlessly on a single processor
17 model, the same test may violate memory coherence rules when run on a multiprocessor model.
18 Finally, the creation of highly deterministic code sequences, such as sequences that execute *if*
19 *then else* statements and other conditional control breaks, can be problematic in dynamically
20 generated tests. The present invention addresses the limitations of current-technology dynamic
21 psuedo-random test pattern generators, which currently select and generate instructions based
22 only upon current machine state. The present invention thus provides a better functional

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1 verification test of some processors, by taking into account machine state, resource availability,
2 and instruction grouping rules in selecting and generating pseudo-random test stimuli. The
3 present invention is a method and apparatus that generates tests that verify that a processor
4 system under test properly executes two or more instructions issued and executed in parallel.
5 The present invention generates tests by dynamically tracking selected system resources of a
6 golden model and by selecting and scheduling instructions for simultaneous execution on the
7 golden model based upon current and future system resource availability, current architectural
8 state of the golden model, and the instruction grouping rules and other architecturally-related
9 rules of the golden model and the processor system under test. The present invention simulates
10 the parallel execution of valid groups instructions, and then updates the architectural state of the
11 golden model. The present invention outputs a test that includes groups of instructions
12 designated for parallel execution on the processor system under test, plus information regarding
13 the correct intermediate states of selected system resources during the test, which enables the
14 user to compare the test results obtained when the test is run on a processor system under test
15 with results obtained when the test is run on a golden model.

The present invention is a method and apparatus that dynamically generates tests that can be used to verify that a processor system under test properly executes two or more instructions issued and executed in parallel. The present invention includes a user preference queue, a rules table, plurality of resource-related data structures, an instruction packer, and an instruction generator and simulator. The user preference queue has a number of entries, each of which comprises an instruction to be tested, a group or tree of instructions to be tested, or a test generator control command. The resource-related data structures comprise information such as actual and/or predicted past state, present state, and future state of selected system resources. In this specification the term “system resources” is defined to include both architectural resources and conceptual resources. Architectural resources include resources like the architectural state of the processor (as defined by the state of specific registers), other registers, the load/store buffer, and the like. The term “conceptual resources” refers to resources that may not actually exist within the architectural state of the machine under test, but instead represent a simple way to represent complex interactions, such as whether or not a branch instruction is pending, or the usage of various units over time, or estimated bus traffic at a particular point in time.

The instruction packer creates a very long instruction word that generally comprises a packet or bundle of two or more instructions valid for parallel execution by the processor under test. The instruction packer selects instructions from the entries in the user preference queue, based upon resource availability as indicated by the resource-related data structures and the architecturally-related instruction grouping rules appropriate for the golden model and the processor system under test. In one mode, the instruction packer selects a first instruction from

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1 an instruction tree in the user preference queue. The instruction packer then selects a second
2 instruction to be packed into one VLIW packet with the first instruction by eliminating
3 instructions in the instruction tree that are ineligible for selection, either because those
4 instructions require a resource that a resource-related data structure indicates is unavailable, or
5 because they require a resource that will be utilized by the first instruction selected and cannot be
6 shared between instructions within a VLIW packet, or because they conflict with the instruction
7 grouping rules appropriate for the golden model and the processor system under test. The
8 instruction packer continues selecting instructions in this manner, by first defining potential
9 groups of instructions valid for selection and then selecting instructions from those groups, until
10 the instruction packer has selected a group of N instructions, where N is the maximum number of
11 instructions that the golden model and the processor system under test can execute in parallel, or
12 until there are no more instructions in the instruction tree that can be validly selected.

13 In another mode, the instruction packer selects instructions in order, from an ordered list
14 that the user provides and that is loaded into the user preference queue. In this mode, the
15 instruction packer selects instructions for parallel execution in the order specified by the user, but
16 stops packing instructions into a VLIW word if an instruction specified by the user cannot be
17 executed in parallel with previously selected instructions, because of resource unavailability,
18 conflicting resources with previously selected instructions, or violations of the instruction
19 grouping rules. In this case, the instruction packer either packs “no operation” instructions into
20 the remaining slots of the VLIW packet, or simply issues the VLIW word “as is” if the processor
21 architecture allows VLIW packets of varying lengths and formats.

22 The present invention marks instructions that have been packed into a VLIW packet to

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indicate that the instructions should be executed in parallel. The instruction generator and simulator generates the instructions selected by the instruction packer, and then simulates the execution of the instructions on the golden model. The present invention updates the appropriate resource-related data structures that correspond to the system resources utilized by the instruction. The present invention evaluates the architectural state of the golden model and updates the appropriate resource-related data structures.

7

Consequently, the *lungs* are the *respiratory organs* of the *body*.

BRIEF DESCRIPTION OF THE DRAWINGS

To further aid in understanding the invention, the attached drawings help illustrate specific features of the invention and the following is a brief description of the attached drawings:

FIG. 1 shows a typical networked computer environment.

FIG. 2 shows a block diagram of a hypothetical VLIW processor architecture and its corresponding VLIW instruction format.

FIG. 3 shows the major components of the present invention and their high-level interaction with each other.

FIGs. 4A and 4B combine to form a flowchart that shows the control and operational flow of the present invention as it creates and conducts functional verification tests.

1 **DETAILED DESCRIPTION OF THE INVENTION**

2 The present invention is a method and apparatus that enables a processor developer to
3 verify that a processor under test properly executes two or more instructions issued and executed
4 in parallel. As described in detail herein, the present invention allows for a robust verification of
5 the parallel execution capabilities of VLIW and other complex processor systems because the
6 present invention generates a processor test while tracking both system resources and the
7 architectural state of the processor golden model. The present invention selects instructions for
8 generation based upon resource availability, processor state, and processor instruction grouping
9 rules. The present invention packs those instructions into a valid very long instruction word and
10 then simulates the execution of the VLIW by the processor golden model. The present invention
11 provides the processor developer with a test comprising a set of pseudo-randomly generated
12 instructions that include instruction packets appropriate for parallel execution, plus time-based
13 intermediate state information produced when those instructions are executed on a golden model,
14 that can then be run on the processor under test for comparison and verification.

15 This disclosure describes numerous specific details that include specific hardware and
16 software structures and example instruction streams in order to provide a thorough understanding
17 of the present invention. One skilled in the art will appreciate that one may practice the present
18 invention without these specific details. In addition, other than the examples provided herein,
19 details concerning the architecture and design rules associated with current advanced VLIW and
20 other parallel issue and/or execution-capable processors are not provided in this disclosure to
21 avoid obfuscation of the present invention. Those skilled in the art will understand that reference
22 herein to processor implementation rules refers to the manufacturer's rules detailed in designers'

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1 reference guides supplied by processor manufacturers, such as Texas Instruments' Instruction Set
2 Reference Guide for the TMS320C62xx CPU, Texas Instruments (July 1997), which is
3 incorporated into this specification by reference for all purposes.

4 The present invention is preferably practiced in the context of a standalone or networked
5 personal computer test setup such as that depicted in FIG. 1. In FIG. 1, typical network 100
6 includes one or more computer workstations 102 networked together via network connection
7 104, which is controlled by network controller 106. The network 100 may also include various
8 peripheral devices, such as network storage device 108 and one or more printers (not shown in
9 FIG. 1). Typical computer workstation 102 includes computer 112, internal storage media such
10 as RAM 118, external storage media such as a floppy disk 114, and various interface devices
11 such as a mouse 116, a monitor 120, and a keyboard 122. Although a particular computer may
12 only have some of the units illustrated in FIG. 1, or may have additional components not shown,
13 most computers will include at least the units shown.

14 In the embodiment described herein, the present invention is implemented in the C++
15 programming language. C++ is a compiled language, that is, programs are written in a human-
16 readable script and this script is then provided to another program called a compiler, which
17 generates a machine-readable numeric code that can be loaded into, and directly executed by, a
18 computer. Those skilled in the art are very familiar with C++, and many articles and texts are
19 available which describe the language in detail. While the exemplary embodiment detailed
20 herein is described using C++ code fragments and pseudo-code, those skilled in the art will
21 understand that the concepts and techniques disclosed herein can be practiced by test designers
22 and operators using any higher-order programming language, such as Java, without departing

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1 from the present invention.

2 FIG. 2 is a block diagram showing a hypothetical VLIW processor 150 having two
3 floating point units 154, 156, an integer arithmetic logic unit 158, a branch processor 160, and a
4 load/store unit 162. VLIW processor 150 also includes an instruction issue unit 152 and a
5 register file 164. FIG. 2 also shows a very long instruction word format 130 for hypothetical
6 VLIW processor 150. As shown in FIG. 2, the instruction word format 130 includes fixed slots
7 for five RISC-like instructions: a floating point addition instruction 132, a floating point
8 multiplication instruction 134, an integer arithmetic instruction 136, a branch instruction 138,
9 and a load/store instruction 140. Those skilled in the art will recognize that FIG. 2 shows a
10 highly simplified, hypothetical case only. For example, rather than having fixed “slots” and
11 fixed-length instruction words, some VLIW processors are much more complex and may utilize
12 instruction words of varying lengths, comprising one or more simple instructions that do not
13 reside in fixed slots, but can be packed in any order. The intention of FIG. 2 is to demonstrate
14 that a VLIW instruction comprises a group or packet of independent, RISC-like instructions that
15 are issued in parallel to multiple independent execution units within the processor. The
16 architecture of the processor thus dictates what kinds of instructions can be grouped together and
17 executed in parallel. The hypothetical processor shown in FIG. 2 can execute simultaneously
18 one floating point addition instruction, one floating point multiplication instruction, one integer
19 arithmetic instruction, one branch instruction, and a load/store instruction, as long as the
20 instructions all utilize different local destination registers.

21 FIG. 3 is a high-level functional block diagram of the test generation apparatus of the
22 present invention. As shown in FIG. 3, the present invention includes a user interface 202, an

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1 inputter 204, a user preference queue 206, an instruction packer 208, a rules table 209, a set of
2 resource-related data structures 210, a template generator 212, one or more templates 214, a
3 mode controller 220, an instruction generator and simulator 216, and an output generator 218.

4 The user interface 202 allows users of the present invention to specify the contents,
5 preferences, and control information required to create a functional verification test of a
6 simulated processor or processor system. In a preferred embodiment, the user interface is a
7 graphical, interactive user interface wherein the user can specify the types of instructions to be
8 simulated by selecting from a menu of instruction choices. In addition, the user can specify test
9 generation preferences, such as whether instructions are to be generated using a biased
10 instruction tree or an ordered instruction list, for example, or whether iterative loops should be
11 inserted, how many instructions can be executed in parallel, whether certain instructions should
12 be executed in parallel with others, or whether the generator should insert and run macros
13 between instructions. Those skilled in the art are familiar with the types of instructions and
14 typical generation controls necessary for the dynamic generation of biased pseudo-random test
15 patterns for processor verification, and therefore further detail regarding instruction selection and
16 generation preferences is not provided herein. In addition, those skilled in the art will recognize
17 that a graphical user interface is optional; advanced users may provide inputs to the present
18 invention using other input methods, such as creating and providing an input text file that
19 contains the necessary instruction generation information.

20 The user interface 202 also enables the user to specify test generation controls that
21 control the generation mode and dictate the user's controls for specific instructions. For
22 example, in a preferred embodiment, the user can assign specific registers to be source registers

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1 or destination registers. Alternatively, the user can assign a specific initial source or destination
2 value for registers and memory locations. Users can specify specific addresses as target
3 addresses for branch instructions or memory operations. Those skilled in the art will recognize
4 that current dynamic pseudo-random test pattern generators generally provide similar instruction
5 and test generation controls, and therefore, further detail regarding the capabilities of the present
6 invention to provide the user with control flexibility and options regarding dynamically
7 generated and executed instructions is not provided here.

8 The inputter 204 accepts test content, preference, and control information from the user
9 via the user interface 202, and adds that information to the user preference queue 206 and the
10 mode controller 220. Each entry in the user preference queue 206 is an instruction, a group/tree
11 of instructions, or a generator command. If the user has indicated that an ordered list of
12 instructions is to be generated and simulated, then the inputter puts that list into the user
13 preference queue in the order specified. If, on the other hand, the user has indicated that some
14 number of instructions are to be generated randomly, then the inputter adds an entire tree of
15 instructions, which may or may not be biased by the user. When the user preference queue 206
16 shrinks below a threshold, additional elements are added by the inputter 204.

17 The operation of the mode controller 220 is described in detail in copending patent
18 application, U.S. Patent App. Ser. No. _____, filed 10.11.00 (10 November 2000)
19 (docket number 62061.0103), now U.S. Pat. No. _____, entitled “Method and
20 Apparatus for Static Test Pattern Generation Within a Dynamic Pseudo-random Test Program
21 Generation Framework,” (hereinafter, the “Static/Dynamic Generator Patent”) which is
22 incorporated by reference into this specification for all purposes. In addition, the Static/Dynamic

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1 Generator Patent also describes the use of templates 214 and the operation of the test generator in
2 both sequential mode and dynamic mode, and details regarding templates and the test generator
3 operating modes are not repeated herein. While the present invention makes use of templates as
4 described in the Static/Dynamic Generator Patent, the special sequential operating mode of the
5 test generator described in the Static/Dynamic Generator Patent does not apply to the present
6 invention. For the purposes of this disclosure, the reader should assume that the test generator is
7 always operating in dynamic mode.

8 Returning to FIG. 3, information from the user preference queue 206, the resource-related
9 data structures 210, the rules table 209, and existing templates 214 is combined in the instruction
10 packer 208 to create sequences of instructions or groups of parallel instructions for generation
11 and simulation. As explained in further detail below, the resource-related data structures 210 are
12 data structures that are created, maintained, and updated to track the actual and/or predicted past
13 state, present state, and future state of selected system resources. In this specification the term
14 “system resources” is defined to include both architectural resources and conceptual resources.
15 Architectural resources include resources like the architectural state of the processor (as defined
16 by the state of specific registers), other registers, the load/store buffer, and the like. The term
17 “conceptual resources” refers to resources that may not actually exist within the architectural
18 state of the machine under test, but instead represent a simple way to represent complex
19 interactions, such as whether or not a branch instruction is pending, or the usage of various
20 execution units over time, or estimated bus traffic at a particular point in time. Practitioners of
21 the present invention may wish to adopt the tracking methodologies and approaches described in
22 detail in copending patent application, U.S. Patent App. Ser. No. _____, filed

62061.0105

1 10.11.00 (10 November 2000) (docket number 62061.0106), now U.S. Pat. No.
2 _____, entitled "Method and Apparatus that Tracks Processor Resources in a
3 Dynamic Pseudo-Random Test Program Generator," (hereinafter, the "Resource Tracking
4 Patent") which is incorporated by reference into this specification for all purposes, to identify
5 system resources appropriate for tracking and to track those resources.

6 The instruction packer 208 uses the resource-related data structures to determine whether
7 resources are currently available, or will be available, when they are needed by specific
8 instructions. Instructions using resources that are either currently in use, or will be in use when
9 they are required are not eligible to be selected and scheduled by the instruction packer 208.

10 The rules table 209 comprises a table of instruction grouping rules, as dictated by the
11 architecture of the processor under test. For example, the rules table 209 for the hypothetical
12 VLIW processor shown in FIG. 2 would indicate that two floating point addition instructions
13 cannot be issued and executed in parallel. Likewise, two branch instructions, two integer
14 arithmetic instructions, or two load/store instructions cannot be packed into the same VLIW
15 group. In a preferred embodiment, the rules table 209 may also include other architecturally-
16 related information useful to the instruction packer, such as the number of processor cycles each
17 individual execution unit requires to execute an instruction, or whether the processor is capable
18 of handling VLIWs of varying lengths, or whether the instruction issue unit can issue
19 instructions to selected idle execution units while others are still operating on previously issued
20 instructions, or whether there are restrictions on register usage by instructions within a single
21 VLIW. Those skilled in the art are very familiar with these architecturally-dictated design rules
22 published by processor manufacturers, and the need to adhere to those rules when developing

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1 new processor systems utilizing the architectural approaches and limitations of existing
2 processors.

3 In a preferred embodiment, the instruction packer 208 selects instructions from the user
4 preference queue 206 and packs them into VLIW groups in two different ways: either randomly,
5 using an instruction tree, or consecutively, according to the order specified by the user. Each
6 instruction selection methodology is explained below.

7 If the user has specified, through the user interface, that some number of instructions
8 should be generated randomly, then the present invention will place an instruction tree into the
9 user preference queue 206. The instruction packer 208 selects a first instruction that can be
10 executed, based upon the current system state information and resource availability information
11 contained within the relevant resource-related data structures 210. The instruction packer 208
12 then selects a group of potentially valid instructions in the user preference queue that can be
13 selected next by eliminating all instructions that are ineligible for selection. For example,
14 instructions within the instruction tree are ineligible for selection if they cannot be executed in
15 parallel with the first instruction selected, as indicated by the rules table 209. Instructions are
16 also ineligible for selection if their resource needs conflict with the first instruction selected, such
17 as might occur if a potential instruction needs a destination register that the first selected
18 instruction will be using. Those skilled in the art will understand that resource conflicts will be
19 ordinarily be dictated by the processor architecture, just as a processor's instruction grouping
20 rules are dictated by the architecture. For example, some architectures may allow two
21 instructions within the same VLIW packet to utilize the same register if it is a source register, but
22 will not allow two instructions to use the same destination register. Others may prohibit all

62061.0105

1 forms of register sharing. Practitioners of the present invention will thus customize the resource
2 conflicts rules implemented in a specific embodiment as required to reflect the architectural
3 requirements and rules of the processor under test.

4 After the instruction packer 208 eliminates all ineligible instructions from the instruction
5 tree, the instruction packer 208 then selects a second instruction for execution in parallel with the
6 first instruction. The instruction packer 208 continues in this manner, repeating the elimination-
7 and-select process by eliminating instructions that utilize either a system resource that conflicts
8 with any previously selected instruction, or that cannot be executed in parallel with any
9 previously selected instruction. The selection process ends when either the maximum number of
10 instructions has been selected (five, in the case of the hypothetical VLIW processor shown in
11 FIG. 2), or no more instructions from the instruction tree are eligible for selection. In the latter
12 case, if the VLIW group is not completely packed and the processor architecture requires all
13 VLIW packets to be of a specific length and format, the instruction packer will fill the remaining
14 slots with “no operation” instructions. Alternatively, if the processor architecture allows VLIW
15 packets of varying lengths, “no operation” instructions may not be required and the VLIW
16 packet can continue through the process as is.

17 When the user has specified that a specific listing of instructions are to be executed in
18 parallel by providing an ordered instruction list to the present invention via the user interface, the
19 instruction packer 208 follows that sequence, to the extent that the user’s instruction sequence
20 comprises a group of instructions that can be validly executed in parallel. In other words, the
21 instruction packer 208 selects the user’s first specified instruction from the user preference queue
22 206 if system resources are available, then selects the user’s second specified instruction if

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1 system resources are available and the user's second specified instruction can be validly grouped
2 with the first instruction, according to the processor's instruction grouping rules. The instruction
3 packer 208 then selects the user's third specified instruction, assuming it does not utilize
4 resources that conflict with the first and second instructions and can be validly grouped with the
5 first and second instructions, and so forth. When the instruction packer 208 encounters an
6 instruction that is ineligible for execution, either because of conflicting resources or because of
7 conflicting grouping rules, the instruction packer 208 stops selecting instructions for a given
8 VLIW packet, and either issues the VLIW packet as is, or fills the remaining slots with "no
9 operation" instructions if required by the processor architecture. When the first instruction on a
10 user's ordered list cannot be selected because of conflicting resources, the instruction packer
11 selects one or more "no operation" instructions until the required resource becomes free and the
12 instruction can be validly selected and packed into a VLIW bundle.

13 For example, assume that the user is testing a processor system having an architecture
14 like the hypothetical VLIW processor shown in FIG. 2. The user has therefore specified that up
15 to five instructions can be packed into one very long instruction word for simulation. Also
16 assume, for this example, that the user has specified that 100 instructions are to be randomly
17 generated for the test.

18 The present invention places an instruction tree into the user preference queue 206. The
19 instruction packer 208 checks the resource-related data structures 210, selects a first instruction
20 based upon resource availability, and places the instruction into the proper position in the VLIW
21 instruction format as defined by the processor's instruction rules. Assume, for this example, that
22 the first instruction selected is a floating point addition instruction that will require operands A

62061.0105

1 and B and registers 1, 2, and 3.

2 For simplicity, we will also assume for this example that the hypothetical VLIW
3 processor does not allow any resource sharing. In this case, the instruction packer 208 then
4 “marks out” all instructions within the tree that require operands A and B and registers 1, 2, and
5 3, and additionally, all other instructions in the tree that must be executed by the processor’s
6 floating point addition execution unit. The instruction packer 208 then selects a second
7 instruction from the remaining instructions in the tree. The second instruction must meet the
8 same requirements as the floating point instruction selected as the first instruction: all system
9 resources required to execute the second instruction must be currently free, the second
10 instruction may not utilize the same system resources required by the instruction already
11 selected, and it must be an instruction that can be validly executed in parallel with the floating
12 point instruction. Returning to the hypothetical VLIW processor shown in FIG. 2, if the
13 instruction packer selects, as the first instruction, a floating point addition instruction that will
14 require operands A and B and registers 1, 2, and 3, a valid second instruction might be a floating
15 point multiplication instruction using operands D and E and registers 4, 5, and 6. The instruction
16 packer would not select another floating point addition instruction, because that selection would
17 violate the processor’s instruction grouping rules. Similarly, the instruction packer would not
18 select a load/store instruction or a branch instruction involving operands A or B, or any of
19 registers 1, 2, or 3, because those system resources will be in use and tied up for some number of
20 cycles by the floating point instruction selected as instruction number one. After a second
21 instruction is selected, the instruction packer selects a third instruction, and so forth, until (in this
22 example) either all five instruction slots are filled, or there are no remaining potentially valid

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1 instructions remaining in the original instruction tree loaded into the user preference queue.

2 After the instructions are selected and packed into the VLIW bundle by the instruction
3 packer 208, the template generator 212 generates a template 214 corresponding to each
4 instruction. In this specification, a template 214 is a data structure that contains an instruction,
5 plus all preferences and data required to execute the instruction. The template for each
6 instruction in a VLIW packet also indicates that it is to be executed in parallel with other
7 instructions, in the manner specified by the processor's design rules.

8 For example, some VLIW processors utilize a bit in the instruction that indicates that the
9 instruction is to be issued and executed in parallel with whatever instruction immediately follows
10 it. The instruction that follows may also have that bit set, indicating that the instruction that
11 follows it should also be issued and executed at the same time as the previous two instructions,
12 and so on. The processor "finds" the last instruction in each group designated for parallel issue
13 and execution because the last instruction does not have the parallel instruction bit set, or
14 alternatively, includes another indication that it is the last instruction in a parallel execution
15 group.

16 Other VLIW processors may require an indication in the first instruction in a group
17 designated for parallel execution that the next "N" instructions should be fetched, issued, and
18 executed simultaneously. These parallel execution rules are defined by the processor architect,
19 in the same manner as the instruction grouping rules discussed above. Those skilled in the art
20 are familiar with the various techniques processor designers use to designate instructions for
21 parallel execution, and practitioners of the present invention that are adapting the present
22 invention for use with various VLIW architectures will understand how to build templates that

62061.0105

1 include the proper indications for parallel execution on a processor under test designed in
2 accordance with a specific architecture.

3 After templates 214 are created, the instructions corresponding to the templates are
4 generated and then simulated. The instruction generator and simulator 216 converts each
5 template 214 into an instruction for the golden model. In a preferred embodiment, this process
6 involves translating the instruction into assembly language or binary, resolving all the
7 instruction's subfields, and initializing any necessary resources to create a valid instruction. The
8 instruction generator and simulator 216 then either calculates or predicts current and future
9 resource utilization as described in further detail below and updates the appropriate resource-
10 related data structure 210. The instruction generator and simulator 216 initiates a step function
11 of the architecturally correct golden model and sends the outstanding instructions to the golden
12 model, which simulates the parallel execution of the instructions and updates its state registers
13 accordingly. The instruction generator and simulator 216 assesses the architectural state of the
14 golden model as a function of time (processor cycles) and updates the appropriate resource-
15 related data structures 210 in preparation for the next iteration of the instruction selection
16 process, and for utilization by the output generator 218, as described below.

17 The output generator 218 generates a machine readable output file containing the test
18 program. The output test file contains the starting state for each component in the system, the
19 commands executed as a function of time, and the intermediate and final states of the golden
20 model as a function of time. Users can then run the output test file on a processor system under
21 test, which provides the same test stimulus to the system under test as was provided to the golden
22 mode. Users then compare the time-based intermediate and final states of the system under test

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1 with the known correct time-based intermediate and final states of the golden model, to verify
2 the functionality of the device or system under test.

3 FIGs. 4A and 4B show a flowchart that illustrates the control and operational flow of the
4 present invention as it creates functional verification tests. At 302, the test operator provides the
5 test inputs (test content, control, and preference information as described above), which are
6 added to the user preference queue at 306 as required by 304. At 308, the instruction packer
7 interfaces with the user preference queue 306, the resource-related data structures represented in
8 FIG. 4A at 312, 314, and 316, and the processor grouping rules table at 309. Using the FIG. 2
9 VLIW processor as an example, at 308, the instruction packer selects five instructions to be
10 packed together into a VLIW in accordance with the procedure described above. These five
11 instructions are then sent in a group to the template generator, which at 310, creates a template
12 for each instruction in the VLIW that is marked for parallel execution in accordance with the
13 processor's architectural rules, as described above. Therefore, continuing with the hypothetical
14 VLIW processor as an example, the template generator might create the following group of
15 templates corresponding to the five possible instructions packed into the VLIW as follows:

Template No.	Program Counter	Template contents
1	1000	Floating point addition instruction and associated information, marked for parallel execution with following instruction
2	1001	Floating point multiplication instruction and associated information, marked for parallel execution with the following instruction
3	1002	Integer addition instruction and associated information, marked for parallel execution with the following instruction
4	1003	Branch instruction and associated information, marked for parallel execution with the following instruction
5	1004	Load/Store instruction and associated information, not marked for parallel execution

62061.0105

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2 After the group of templates is created at 310, the present invention jumps to the main
3 loop of the test generator 320, shown in FIG. 4B, and checks the operational mode at 326. As
4 the reader will recall, the test generator will always be in dynamic mode when implementing
5 parallel scheduling and simulation of instructions as described herein.

6 At 328, the instructions corresponding to all outstanding templates are generated at 328,
7 resources are calculated 330, estimated 332, the appropriate resource-related data structures are
8 updated at 312 and 314, and the group of instructions are then sent to the golden model at 334 for
9 simulation. The present invention evaluates the state of the golden model and records that state,
10 as a function of time, for the output file. The present invention also updates the appropriate
11 resource-related data structures that correspond to the golden model architectural state in
12 preparation for the next instruction selection and packing step.

13 At the next check at 324, a template will not exist at the current program counter, and the
14 present invention will return to the instruction packer, which then selects a new group of
15 instructions for parallel execution using the procedure described above, and the entire process
16 repeats until the end of the test.

17 As described above, the present invention is also capable of generating tests where the
18 user can specify a specifically ordered group of instructions to be generated for parallel
19 execution. In that case, the user provides an ordered list of instructions via the user interface,
20 rather than an instruction tree. In this case, as described above, the instruction packer selects
21 instructions from the list in the user preference queue in the order specified by the user, assuming
22 that system resources are available and the instructions listed do not violate the processor's

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1 instruction grouping rules. Groups of instructions are sent to the template generator, and groups
2 of templates are created at 310 in the same manner as that described above. After a group of
3 templates is created for a VLIW packed by the instruction packer, the present invention jumps to
4 the main loop 320, and generates and simulates the instructions as described above. Following
5 simulation of each VLIW packet, the present invention will return to the instruction packer at
6 308, which will then pack the next VLIW group using the instructions in the user's list, picking
7 up where it left off with the previous VLIW. The present invention will continue packing VLIW
8 instructions and creating template sequences in this manner, as long as nonconflicting resources
9 are available and as long as the processor's instruction grouping rules are not violated. If the
10 present invention encounters an instruction on the user's list that cannot be selected due to (for
11 example) unavailable system resources, in one embodiment, the instruction packer simply packs
12 one or more "no operation" instructions into VLIW groups until the resource becomes available
13 and the instruction can be packed, generated, and simulated.

14 **Resource tracking.**

15 As described above, the present invention selects instructions appropriate for parallel
16 execution by, among other things, examining the available system resources and selecting only
17 those instructions that can be executed because the system resources they require are or will be
18 free at the appropriate time. After groups of instructions are generated at 328 in FIG. 4B,
19 resource usage is reevaluated at 330 and 332, and the appropriate resource-related data structures
20 are updated at 312 and 314. These updated resource-related data structures affect the selection of
21 the next group of instructions that the instruction packer selects for the next VLIW packet to be
22 generated and simulated.

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1 The present invention tracks the current state of architectural resources, such as
2 individual registers, the load/store buffer, the architectural state of the processor as defined by a
3 specific subset of registers, and the like, as a function of time. The present invention also tracks
4 the utilization of the various execution units within the processor, again as a function of time.
5 For example, in an embodiment of the present invention customized to generate a test for a
6 processor system designed according to Texas Instruments' TMS320C62xx architecture, floating
7 point instructions require four processor cycles to complete. The present invention tracks the
8 utilization of the floating point execution unit, and the instruction packer will only select a
9 floating point instruction when the floating point unit is free, as indicated by the relevant
10 floating-point execution unit data structure. Furthermore, when a floating point instruction is
11 packed into a VLIW packet and the corresponding floating point instructions are generated by
12 the instruction generator, the present invention designates the floating point execution unit as
13 unavailable for four processor cycles. Assuming a VLIW group is packed and issued during
14 each processor cycle, the instruction packer is thus barred from selecting another floating point
15 instruction until four processor cycles have elapsed, at which point the floating point unit
16 becomes available. Similarly, the destination register(s) that the floating point instruction uses
17 are also unavailable for four processor cycles, after which they will be updated to reflect the
18 values determined by the execution of the floating point instruction. The instruction packer is
19 thus barred from selecting another instruction that requires the same destination registers used by
20 the floating point instruction until four processor cycles have elapsed. Those skilled in the art
21 will recognize that, while neither the floating point execution unit utilization nor the values in or
22 utilization of specific general purpose registers is reflected in the defined architectural state

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1 within the golden model, tracking these system resources to aid in the efficient scheduling of test
2 instructions is highly useful.

3 Practitioners of the present invention that are customizing the present invention for a
4 specific processor architecture can glean the information required to track relevant system
5 resources from the programmer's manual provided by the processor's manufacturer. After
6 reading this specification or practicing the present invention, practitioners of the present
7 invention will understand that there are a number of different design approaches that will each
8 accomplish the resource tracking described herein. For example, practitioners of the present
9 invention might include a resource tracker at 330 that examines the type of instruction generated
10 (e.g., a floating point instruction or a branch instruction), turns to a table to determine the number
11 of processor cycles to mark the associated execution unit as "unavailable" (e.g., 4 cycles, in the
12 case of the floating point execution unit or 2 cycles, in the case of the branch unit), and updates
13 the data structure associated with the relevant execution unit to reflect that the execution unit is
14 unavailable for the appropriate number of cycles. Similarly, the same tracker might use the same
15 table to mark the registers and other resources associated with the instruction (identified on the
16 instruction's template) as unavailable during the appropriate number of processor cycles.
17 Practitioners of the present invention might choose to incorporate two pieces of information into
18 the data structure associated with registers: the availability of the register, and the value
19 currently loaded into the register. Alternatively, practitioners might choose to utilize separate
20 data structures for individual register availability and individual register value.

21 When tracking the future state of selected system resources (i.e., unavailability for a
22 specific number of processor cycles), those skilled in the art will recognize that the tracker must

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1 also update the data structures associated with the system resources at the appropriate time to
2 reflect that the resource is now available again, thus indicating to the instruction packer that an
3 instruction that requires the newly-freed resource can now be properly selected and packed into a
4 new VLIW.

5 Unlike the execution unit utilization or specific register utilization or states, some system
6 resources that would be useful to track to maintain efficiency in scheduling instructions cannot
7 be easily tracked. For example, processors typically execute loads and stores from the load/store
8 buffer on a non-interrupt, background basis. Consequently, it is difficult to determine the precise
9 contents of the load/store buffer at a specific point in time, because it is difficult to determine at a
10 specific instance whether pending loads and stores have been written to and from memory.
11 Nevertheless, those skilled in the art can construct a heuristic model that represents a prediction
12 of traffic in the load/store buffer as a function of the number and timing of load/store instructions
13 generated in a specific test. When the predicted traffic through the load/store buffer reaches a
14 certain predetermined threshold, the present invention can update a data structure that
15 corresponds to the load/store buffer to designate the load/store buffer as unavailable. This will
16 prevent the instruction packer from selecting further load/store instructions for packing into
17 further VLIW groups until the load/store traffic drops below the specified threshold, at which
18 time the tracker redesignates the load/store buffer as available. Alternatively, the user may want
19 to specifically test a processor's ability to function properly when the load/store buffer is highly
20 stressed by dense traffic to and from memory. In this case, the data structure corresponding to
21 the load/store buffer would not be marked as unavailable, and the instruction packer would
22 continue to select and pack load/store instructions, but the user would want to continue to

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1 monitor the traffic density in the load/store buffer over time.

2 System resources that practitioners of the present invention may find useful to track,
3 either directly as described in the execution unit example, or by predictive methods as described
4 in the load/store buffer example, include the utilization of various execution units within the
5 system, state and utilization of general or special purpose registers, subfields of general or
6 special purpose registers, instruction and data caches, system bus status, physical memory,
7 virtual memory system page tables, and resources capable of generating system exceptions and
8 interrupts. The reader is referred to the Resource Tracking Patent for details on resource tracking
9 methodologies that can be employed to generate resource-related data structures appropriate for
10 use with the present invention.

11 To summarize, the present invention is a method and apparatus that generates a test that
12 enables the verification that a processor system under test properly executes two or more
13 instructions issued and executed in parallel. The present invention includes a user preference
14 queue, a rules table, plurality of resource-related data structures, an instruction packer, and an
15 instruction generator and simulator. The user preference queue has a number of entries, each of
16 which comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
17 generator control command. The resource-related data structures comprise information such as
18 actual and/or predicted past state, present state, and future state of selected system resources.

19 The instruction packer creates a very long instruction word that can comprise two or
20 more instructions valid for parallel execution by the processor under test. The instruction packer
21 selects instructions from the entries in the user preference queue, based upon resource
22 availability as indicated by the resource-related data structures and the architecturally-related

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1 instruction grouping rules appropriate for the golden model and the processor system under test.
2 The instruction packer also insures that instructions within a single VLIW do not require
3 conflicting system resources.

4 The present invention marks instructions that have been packed into a VLIW to indicate
5 that the instructions should be executed in parallel. The instruction generator and simulator
6 generates the instructions that correspond to each instruction selected by the instruction packer,
7 and then simulates the execution of the instructions on the golden model. The present invention
8 updates the appropriate resource-related data structures that correspond to the system resources
9 utilized by the instruction. The present invention also evaluates the architectural state of the
10 golden model as a function of time and updates the appropriate resource-related data structures.

11 Other embodiments of the invention will be apparent to those skilled in the art after
12 considering this specification or practicing the disclosed invention. The specification and
13 examples above are exemplary only, with the true scope of the invention being indicated by the
14 following claims.

CLAIMS

We claim the following invention:

1 1. A processor verification test apparatus that uses a golden model to generate a test that
2 verifies that a processor system under test properly executes two or more instructions issued and
3 executed in parallel, comprising:

4 a user preference queue that comprises queue entries wherein each queue entry further
5 comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
6 generator control command;

7 a plurality of resource-related data structures, wherein each said resource-related data
8 structure comprises information concerning selected system resources of the golden model,
9 wherein said information comprises one or more of the following: actual past state, actual
10 present state, actual future state, predicted past state, predicted present state, or predicted future
11 state;

12 an instruction packer coupled to said user preference queue and said resource-related data
13 structures, said instruction packer creates a group of N instructions valid for parallel execution
14 by the golden model and the processor system under test, where N equals 1 or more; and

15 an instruction generator and simulator that generates and simulates instructions that
16 correspond to said group of N instructions created by said instruction packer, evaluates the
17 updated architectural state of the golden model, and updates said resource-related data structures.

18

19 2. The apparatus of claim 1, wherein said group of N instructions valid for parallel
20 execution further comprises N instructions that do not utilize common system resources other

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1 than source registers of the golden model or the processor system under test.

2

3 3. The apparatus of claim 1, wherein said instruction packer creates said group of N
4 instructions valid for parallel execution by selecting instructions from an instruction tree in said
5 user preference queue, wherein said instruction packer iteratively creates a group of potentially
6 valid instructions by eliminating instructions ineligible for selection, based upon information
7 indicated by said resource-related data structures and the instruction grouping rules for the
8 golden model and the processor system under test.

9

10 4. The apparatus of claim 3, wherein said group of N instructions further comprises at least
11 a first instruction and a second instruction, wherein said second instruction is selected from said
12 group of potentially valid instructions, and wherein said second instruction further comprises an
13 instruction that does not utilize the same system resources other than source registers utilized by
14 said first instruction.

15

16 5. The apparatus of claim 1, wherein said instruction packer creates said group of N
17 instructions valid for parallel execution by selecting instructions in one of the following ways:
18 by selecting each instruction in the order that said instruction appears in an ordered instruction
19 list in said user preference queue, or by selecting a “no operation” instruction where the next
20 instruction in said ordered instruction list requires unavailable system resources or violates the
21 processor grouping rules.

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1 6. A processor verification test system that uses a golden model to generate a test that
2 verifies that a processor system under test properly executes two or more instructions issued and
3 executed in parallel, comprising:

4 a user preference queue that comprises queue entries wherein each queue entry further
5 comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
6 generator control command;

7 a plurality of resource-related data structures, wherein each said resource-related data
8 structure comprises information concerning selected system resources of the golden model,
9 wherein said information comprises one or more of the following: actual past state, actual
10 present state, actual future state, predicted past state, predicted present state, or predicted future
11 state;

12 an instruction packer coupled to said user preference queue and said resource-related data
13 structures, said instruction packer creates a group of N instructions valid for parallel execution
14 by the golden model and the processor system under test, where N equals 1 or more; and

15 an instruction generator and simulator that generates and simulates instructions that
16 correspond said group of N instructions created by said instruction packer, evaluates the updated
17 architectural state of the golden model, and updates said resource-related data structures.

19 7. The system of claim 6, wherein said group of N instructions valid for parallel execution
20 further comprises N instructions that do not utilize common system resources other than source
21 registers of the golden model or the processor system under test.

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1 8. The system of claim 6, wherein said instruction packer creates said group of N
2 instructions valid for parallel execution by selecting instructions from an instruction tree in said
3 user preference queue, wherein said instruction packer iteratively creates a group of potentially
4 valid instructions by eliminating instructions ineligible for selection, based upon information
5 indicated by said resource-related data structures and the instruction grouping rules for the
6 golden model and the processor system under test.

7

8 9. The system of claim 8, wherein said group of N instructions further comprises at least a
9 first instruction and a second instruction, wherein said second instruction is selected from said
10 group of potentially valid instructions, wherein said second instruction further comprises an
11 instruction that does not utilize the same system resources other than source registers that are
12 utilized by said first instruction.

13

14 10. The system of claim 6, wherein said instruction packer creates said group of N
15 instructions valid for parallel execution by selecting instructions in one of the following ways:
16 by selecting each instruction in the order that said instruction appears in an ordered instruction
17 list in said user preference queue, or by selecting a “no operation” instruction where the next
18 instruction in said ordered instruction list requires unavailable system resources or violates the
19 processor grouping rules.

20

21 11. A method that makes a processor verification test apparatus that uses a golden model to
22 create a test that verifies that a processor system under test properly executes two or more

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1 instructions issued and executed in parallel, comprising:

2 providing a user preference queue that comprises queue entries wherein each queue entry
3 further comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
4 generator control command;

5 providing a plurality of resource-related data structures, wherein each said resource-
6 related data structure comprises information concerning selected system resources of the golden
7 model, wherein said information comprises one or more of the following: actual past state,
8 actual present state, actual future state, predicted past state, predicted present state, or predicted
9 future state;

10 coupling an instruction packer to said user preference queue and said resource-related
11 data structures, said instruction packer creates a group of N instructions valid for parallel
12 execution by the golden model and the processor system under test, where N equals 1 or more;
13 and

14 coupling an instruction generator and simulator to said instruction packer and said
15 resource-related data structures, said instruction generator and simulator generates and simulates
16 instructions that correspond said group of N instructions created by said instruction packer,
17 evaluates the updated architectural state of the golden model, and updates said resource-related
18 data structures.

19

20 12. The method of claim 11, wherein said group of N instructions valid for parallel execution
21 further comprises N instructions that do not utilize common system resources other than source
22 registers of the golden model or the processor system under test.

1

2 13. The method of claim 11, wherein said instruction packer creates said group of N
3 instructions valid for parallel execution by selecting instructions from an instruction tree in said
4 user preference queue, wherein said instruction packer iteratively creates a group of potentially
5 valid instructions by eliminating instructions ineligible for selection, based upon information
6 indicated by said resource-related data structures and the instruction grouping rules for the
7 golden model and the processor system under test.

8

9 14. The method of claim 13, wherein said group of N instructions further comprises at least a
10 first instruction and a second instruction, wherein said second instruction is selected from said
11 group of potentially valid instructions, wherein said second instruction further comprises an
12 instruction that does not utilize the same system resources other than source registers utilized by
13 said first instruction.

14

15 15. The method of claim 11, wherein said instruction packer creates said group of N
16 instructions valid for parallel execution by selecting instructions in one of the following ways:
17 by selecting each instruction in the order that said instruction appears in an ordered instruction
18 list in said user preference queue, or by selecting a “no operation” instruction where the next
19 instruction in said ordered instruction list requires unavailable system resources or violates the
20 processor grouping rules.

21

22 16. A method that generates a test that verifies that a processor system under test properly

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1 executes two or more instructions issued and executed in parallel, comprising:
2 filling a user preference queue with queue entries, wherein each queue entry further
3 comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
4 generator control command;

5 generating a plurality of resource-related data structures, wherein each said resource-
6 related data structure comprises information concerning selected system resources of the golden
7 model, wherein said information comprises one or more of the following: actual past state,
8 actual present state, actual future state, predicted past state, predicted present state, or predicted
9 future state;

10 creating a group of N instructions valid for parallel execution by the golden model and
11 the processor system under test, where N equals 1 or more, by selecting instructions from said
12 queue entries based upon information within said resource-related data structures and the
13 instruction grouping rules for the golden model and the processor system under test; and

14 generating and simulating instructions that correspond said group of N instructions,
15 evaluating the updated architectural state of the golden model, and updating said resource-related
16 data structures.

17
18 17. The method of claim 16, wherein said group of N instructions valid for parallel execution
19 further comprises N instructions that do not utilize common system resources other than source
20 registers of the golden model or the processor system under test.

21
22 18. The method of claim 16, wherein said group of N instructions valid for parallel execution

62061.0105

1 is created by selecting instructions from an instruction tree in said user preference queue, and
2 said method further comprises iteratively creating a group of potentially valid instructions by
3 eliminating instructions ineligible for selection, based upon information within said resource-
4 related data structures and the instruction grouping rules for the golden model and the processor
5 system under test.

6

7 19. The method of claim 18, wherein said group of N instructions further comprises at least a
8 first instruction and a second instruction, wherein said second instruction is selected from said
9 group of potentially valid instructions, wherein said second instruction further comprises an
10 instruction that does not utilize the same system resources other than source registers utilized by
11 said first instruction.

12

13 20. The method of claim 16, wherein creating said group of N instructions valid for parallel
14 execution further comprises selecting instructions in one of the following ways: selecting each
15 instruction in the order that said instruction appears in an ordered instruction list in said user
16 preference queue, or selecting a “no operation” instruction where the next instruction in said
17 ordered instruction list requires unavailable system resources or violates the processor grouping
18 rules.

19

20 21. A program storage device readable by a computer that tangibly embodies a program of
21 instructions executable by the computer to perform a method that generates a test that verifies
22 that a processor system under test properly executes two or more instructions issued and

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1 executed in parallel, comprising:

2 filling a user preference queue with queue entries, wherein each queue entry further
3 comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
4 generator control command;

5 generating a plurality of resource-related data structures, wherein each said resource-
6 related data structure comprises information concerning selected system resources of the golden
7 model, wherein said information comprises one or more of the following: actual past state,
8 actual present state, actual future state, predicted past state, predicted present state, or predicted
9 future state;

10 creating a group of N instructions valid for parallel execution by the golden model and
11 the processor system under test, where N equals 1 or more, by selecting instructions from said
12 queue entries based upon information within said resource-related data structures and the
13 instruction grouping rules for the golden model and the processor system under test; and

14 generating and simulating instructions that correspond said group of N instructions,
15 evaluating the updated architectural state of the golden model, and updating said resource-related
16 data structures.

17

18 22. The program storage device of claim 21, wherein said group of N instructions valid for
19 parallel execution further comprises N instructions that do not utilize common system resources
20 other than source registers of the golden model or the processor system under test.

21

22 23. The program storage device of claim 21, wherein said group of N instructions valid for

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1 parallel execution is created by selecting instructions from an instruction tree in said user
2 preference queue, and said method further comprises iteratively creating a group of potentially
3 valid instructions by eliminating instructions ineligible for selection, based upon information
4 within said resource-related data structures and the instruction grouping rules for the golden
5 model and the processor system under test.

6

7 24. The program storage device of claim 23, wherein said group of N instructions further
8 comprises at least a first instruction and a second instruction, wherein said second instruction is
9 selected from said group of potentially valid instructions, wherein said second instruction further
10 comprises an instruction that does not utilize the same system resources other than source
11 registers utilized by said first instruction.

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25. The program storage device of claim 21, wherein creating said group of N instructions
valid for parallel execution further comprises selecting instructions in one of the following ways:
selecting each instruction in the order that said instruction appears in an ordered instruction list
in said user preference queue, or selecting a “no operation” instruction where the next instruction
in said ordered instruction list requires unavailable system resources or violates the processor
grouping rules.

23

24

25

26

26. A processor verification test apparatus that uses a golden model to generate a test that
verifies that a processor system under test properly executes two or more instructions issued and
executed in parallel, comprising:

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1 a user preference queue that comprises queue entries wherein each queue entry further
2 comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
3 generator control command;

4 a plurality of resource-related data structures, wherein each said resource-related data
5 structure comprises information concerning selected system resources of the golden model,
6 wherein said information comprises one or more of the following: actual past state, actual
7 present state, actual future state, predicted past state, predicted present state, or predicted future
8 state;

9 an instruction packer coupled to said user preference queue and said resource-related data
10 structures, said instruction packer creates a group of N instructions valid for parallel execution
11 by the golden model and the processor system under test, wherein said N instructions do not
12 utilize common system resources other than source registers of the golden model or the processor
13 system under test and where N equals 1 or more, by selecting instructions in one of the following
14 two ways: from an instruction tree in said user preference queue, wherein said instruction packer
15 iteratively creates a group of potentially valid instructions by eliminating instructions ineligible
16 for selection, based upon information indicated by said resource-related data structures and the
17 instruction grouping rules for the golden model and the processor system under test, in which
18 case said group of N instructions further comprises at least a first instruction and a second
19 instruction, wherein said second instruction is selected from said group of potentially valid
20 instructions, and wherein said second instruction further comprises an instruction that does not
21 utilize the same system resources other than source registers utilized by said first instruction, or
22 from an ordered instruction list in said user preference queue, wherein each instruction selected

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1 comprises either the next instruction in said ordered instruction list or a “no operation”
2 instruction if said next instruction in said ordered instruction list requires unavailable system
3 resources or violates the processor grouping rules; and

4 an instruction generator and simulator that generates and simulates instructions that
5 correspond to said group of N instructions created by said instruction packer, evaluates the
6 updated architectural state of the golden model, and updates said resource-related data structures.

7

8 27. A processor verification test system that uses a golden model to generate a test that
9 verifies that a processor system under test properly executes two or more instructions issued and
10 executed in parallel, comprising:

11 a user preference queue that comprises queue entries wherein each queue entry further
12 comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
13 generator control command;

14 a plurality of resource-related data structures, wherein each said resource-related data
15 structure comprises information concerning selected system resources of the golden model,
16 wherein said information comprises one or more of the following: actual past state, actual
17 present state, actual future state, predicted past state, predicted present state, or predicted future
18 state;

19 an instruction packer coupled to said user preference queue and said resource-related data
20 structures, said instruction packer creates a group of N instructions valid for parallel execution
21 by the golden model and the processor system under test, wherein said N instructions do not
22 utilize common system resources other than source registers of the golden model or the processor

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1 system under test and where N equals 1 or more, by selecting instructions in one of the following
2 two ways: from an instruction tree in said user preference queue, wherein said instruction packer
3 iteratively creates a group of potentially valid instructions by eliminating instructions ineligible
4 for selection, based upon information indicated by said resource-related data structures and the
5 instruction grouping rules for the golden model and the processor system under test, in which
6 case said group of N instructions further comprises at least a first instruction and a second
7 instruction, wherein said second instruction is selected from said group of potentially valid
8 instructions, and wherein said second instruction further comprises an instruction that does not
9 utilize the same system resources other than source registers utilized by said first instruction, or
10 from an ordered instruction list in said user preference queue, wherein each instruction selected
11 comprises either the next instruction in said ordered instruction list or a “no operation”
12 instruction if said next instruction in said ordered instruction list requires unavailable system
13 resources or violates the processor grouping rules; and

14 an instruction generator and simulator that generates and simulates instructions that
15 correspond to said group of N instructions created by said instruction packer, evaluates the
16 updated architectural state of the golden model, and updates said resource-related data structures.

17
18 28. A method that makes a processor verification test apparatus that uses a golden model to
19 generate a test that verifies that a processor system under test properly executes two or more
20 instructions issued and executed in parallel, comprising:
21

22 providing a user preference queue that comprises queue entries wherein each queue entry
further comprises an instruction to be tested, a group or tree of instructions to be tested, or a test

62061.0105

1 generator control command;

2 providing a plurality of resource-related data structures, wherein each said resource-
3 related data structure comprises information concerning selected system resources of the golden
4 model, wherein said information comprises one or more of the following: actual past state,
5 actual present state, actual future state, predicted past state, predicted present state, or predicted
6 future state;

7 providing an instruction packer coupled to said user preference queue and said resource-
8 related data structures, said instruction packer creates a group of N instructions valid for parallel
9 execution by the golden model and the processor system under test, wherein said N instructions
10 do not utilize common system resources other than source registers of the golden model or the
11 processor system under test and where N equals 1 or more, by selecting instructions in one of the
12 following two ways: from an instruction tree in said user preference queue, wherein said
13 instruction packer iteratively creates a group of potentially valid instructions by eliminating
14 instructions ineligible for selection, based upon information indicated by said resource-related
15 data structures and the instruction grouping rules for the golden model and the processor system
16 under test, in which case said group of N instructions further comprises at least a first instruction
17 and a second instruction, wherein said second instruction is selected from said group of
18 potentially valid instructions, and wherein said second instruction further comprises an
19 instruction that does not utilize the same system resources other than source registers utilized by
20 said first instruction, or from an ordered instruction list in said user preference queue, wherein
21 each instruction selected comprises either the next instruction in said ordered instruction list or a
22 “no operation” instruction if said next instruction in said ordered instruction list requires

62061.0105

1 unavailable system resources or violates the processor grouping rules; and

2 providing an instruction generator and simulator that generates and simulates instructions
3 that correspond to said group of N instructions created by said instruction packer, evaluates the
4 updated architectural state of the golden model, and updates said resource-related data structures.

5

6 29. A method that uses a golden model to generate a test that verifies that a processor system
7 under test properly executes two or more instructions issued and executed in parallel,
8 comprising:

9 filling a user preference queue that comprises queue entries wherein each queue entry
10 further comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
11 generator control command;

12 generating a plurality of resource-related data structures, wherein each said resource-
13 related data structure comprises information concerning selected system resources of the golden
14 model, wherein said information comprises one or more of the following: actual past state,
15 actual present state, actual future state, predicted past state, predicted present state, or predicted
16 future state;

17 creating a group of N instructions valid for parallel execution by the golden model and
18 the processor system under test using an instruction packer coupled to said user preference queue
19 and said resource-related data structures, wherein said N instructions do not utilize common
20 system resources other than source registers of the golden model or the processor system under
21 test and where N equals 1 or more, by selecting instructions in one of the following two ways:
22 from an instruction tree in said user preference queue, wherein said instruction packer iteratively

62061.0105

1 creates a group of potentially valid instructions by eliminating instructions ineligible for
2 selection, based upon information indicated by said resource-related data structures and the
3 instruction grouping rules for the golden model and the processor system under test, in which
4 case said group of N instructions further comprises at least a first instruction and a second
5 instruction, wherein said second instruction is selected from said group of potentially valid
6 instructions, and wherein said second instruction further comprises an instruction that does not
7 utilize the same system resources other than source registers utilized by said first instruction, or
8 from an ordered instruction list in said user preference queue, wherein each instruction selected
9 comprises either the next instruction in said ordered instruction list or a “no operation”
10 instruction if said next instruction in said ordered instruction list requires unavailable system
11 resources or violates the processor grouping rules; and

12 generating and simulating instructions that correspond to said group of N instructions
13 created by said instruction packer, evaluating the updated architectural state of the golden model,
14 and updating said resource-related data structures.

15
16 30. A program storage device readable by a computer that tangibly embodies a program of
17 instructions executable by the computer to perform a method that uses a golden model to
18 generate a test that verifies that a processor system under test properly executes two or more
19 instructions issued and executed in parallel, comprising:

20 filling a user preference queue that comprises queue entries wherein each queue entry
21 further comprises an instruction to be tested, a group or tree of instructions to be tested, or a test
22 generator control command;

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1 generating a plurality of resource-related data structures, wherein each said resource-
2 related data structure comprises information concerning selected system resources of the golden
3 model, wherein said information comprises one or more of the following: actual past state,
4 actual present state, actual future state, predicted past state, predicted present state, or predicted
5 future state;

6 creating a group of N instructions valid for parallel execution by the golden model and
7 the processor system under test using an instruction packer coupled to said user preference queue
8 and said resource-related data structures, wherein said N instructions do not utilize common
9 system resources other than source registers of the golden model or the processor system under
10 test and where N equals 1 or more, by selecting instructions in one of the following two ways:
11 from an instruction tree in said user preference queue, wherein said instruction packer iteratively
12 creates a group of potentially valid instructions by eliminating instructions ineligible for
13 selection, based upon information indicated by said resource-related data structures and the
14 instruction grouping rules for the golden model and the processor system under test, in which
15 case said group of N instructions further comprises at least a first instruction and a second
16 instruction, wherein said second instruction is selected from said group of potentially valid
17 instructions, and wherein said second instruction further comprises an instruction that does not
18 utilize the same system resources other than source registers utilized by said first instruction, or
19 from an ordered instruction list in said user preference queue, wherein each instruction selected
20 comprises either the next instruction in said ordered instruction list or a “no operation”
21 instruction if said next instruction in said ordered instruction list requires unavailable system
22 resources or violates the processor grouping rules; and

62061.0105

1 generating and simulating instructions that correspond to said group of N instructions
2 created by said instruction packer, evaluating the updated architectural state of the golden model,
3 and updating said resource-related data structures.

4

ABSTRACT

1 A dynamic test generation method and apparatus enabling verification of the parallel
2 instruction execution capabilities of VLIW processor systems is described. The test generator
3 includes a user preference queue, a rules table, plurality of resource-related data structures, an
4 instruction packer, and an instruction generator and simulator. The present invention generates a
5 test by selecting instructions for parallel execution based upon resource availability as indicated
6 by the resource-related data structures and the processor's instruction grouping rules, simulating
7 the parallel execution of the instructions on a golden model, updating the resource-related data
8 structures, and evaluating the updated architectural state of the golden model.

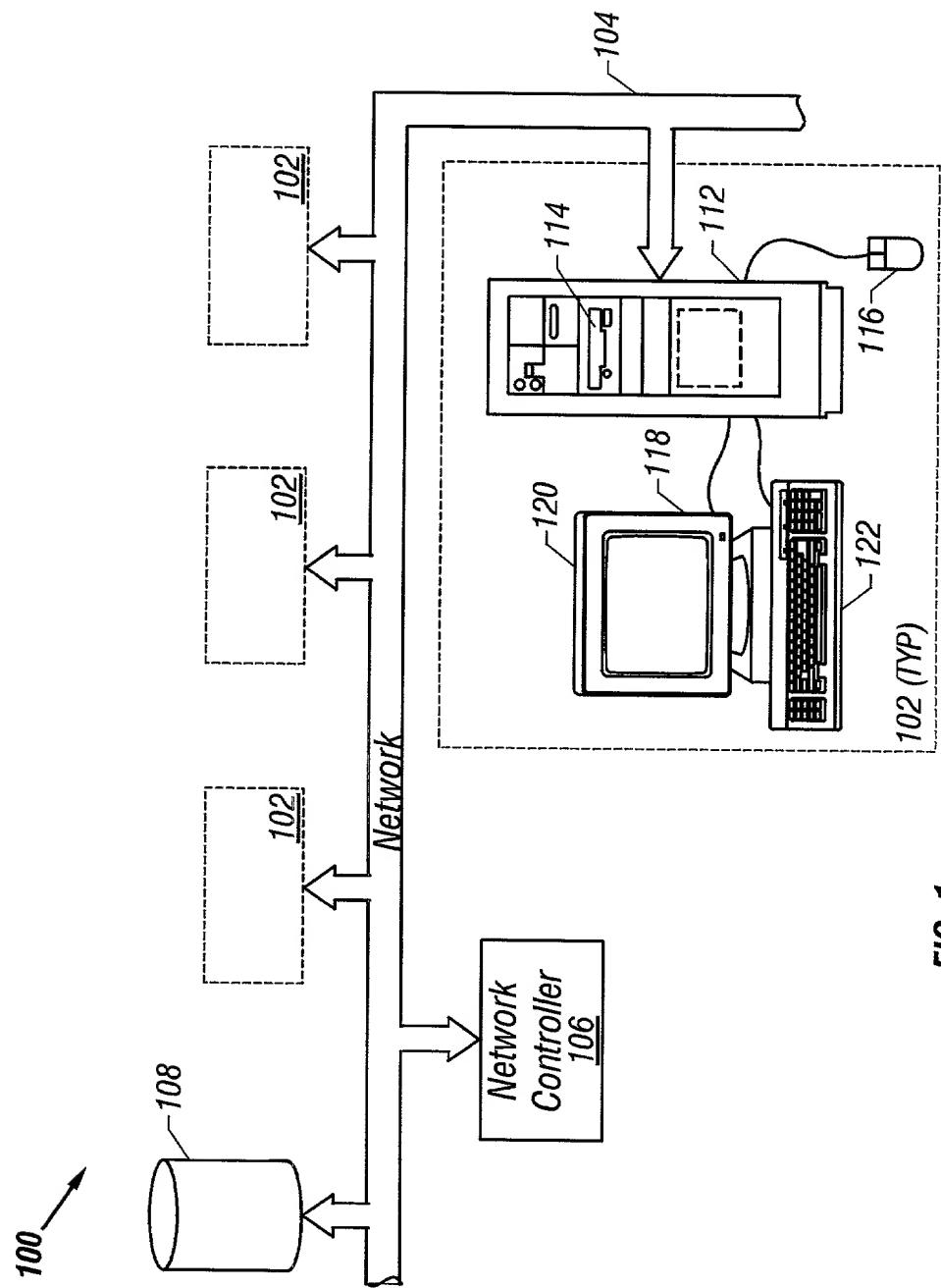


FIG. 1

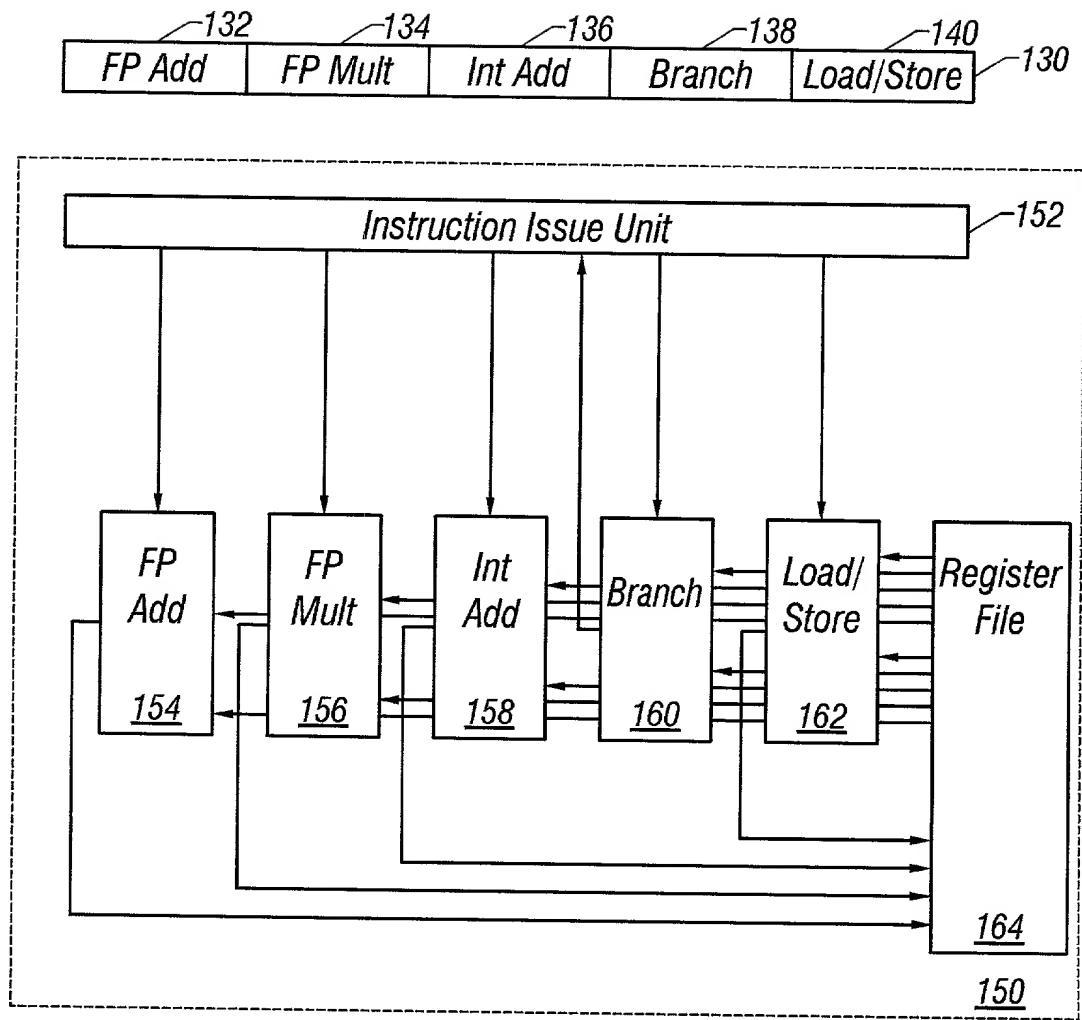


FIG. 2

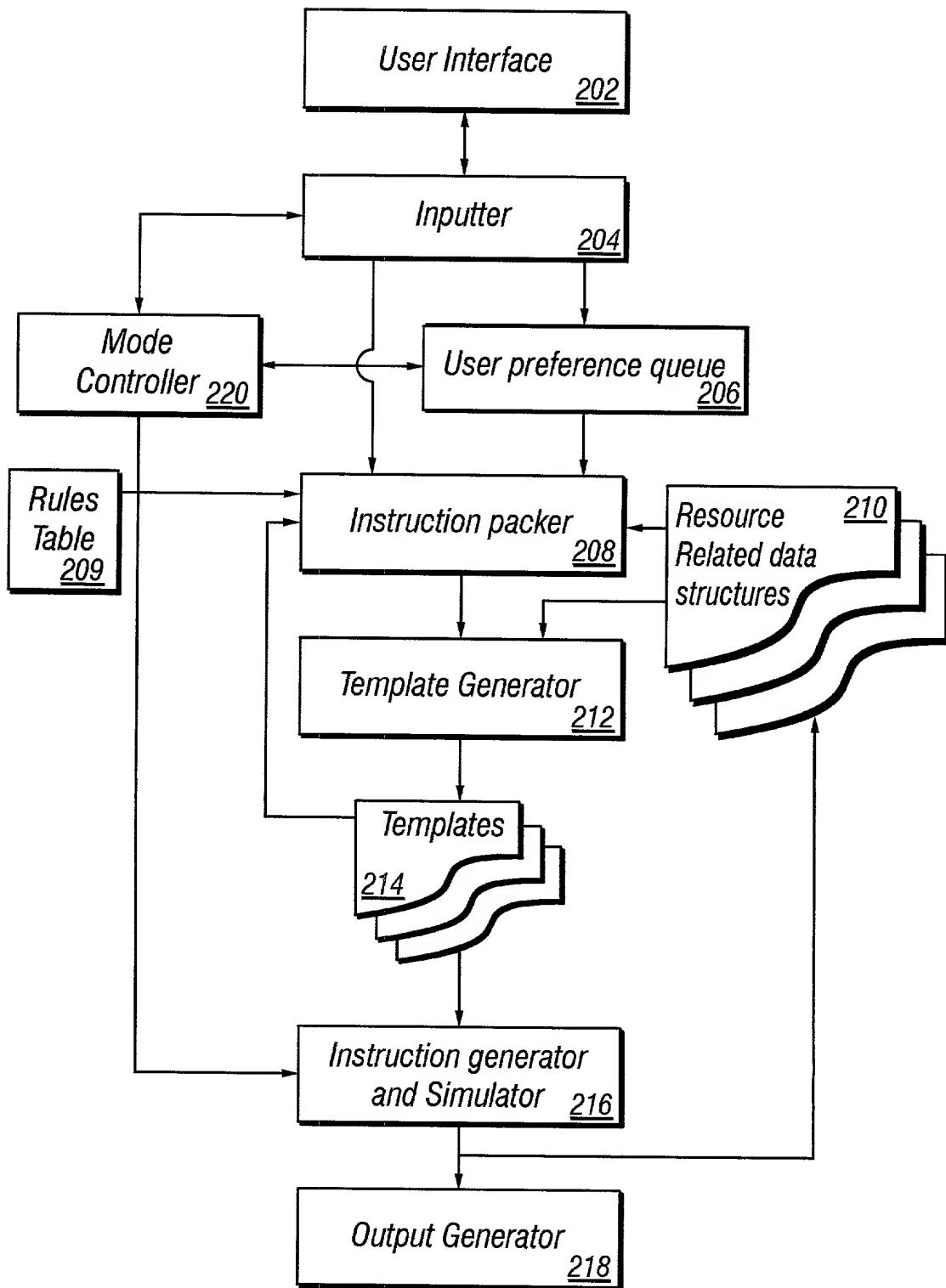


FIG. 3

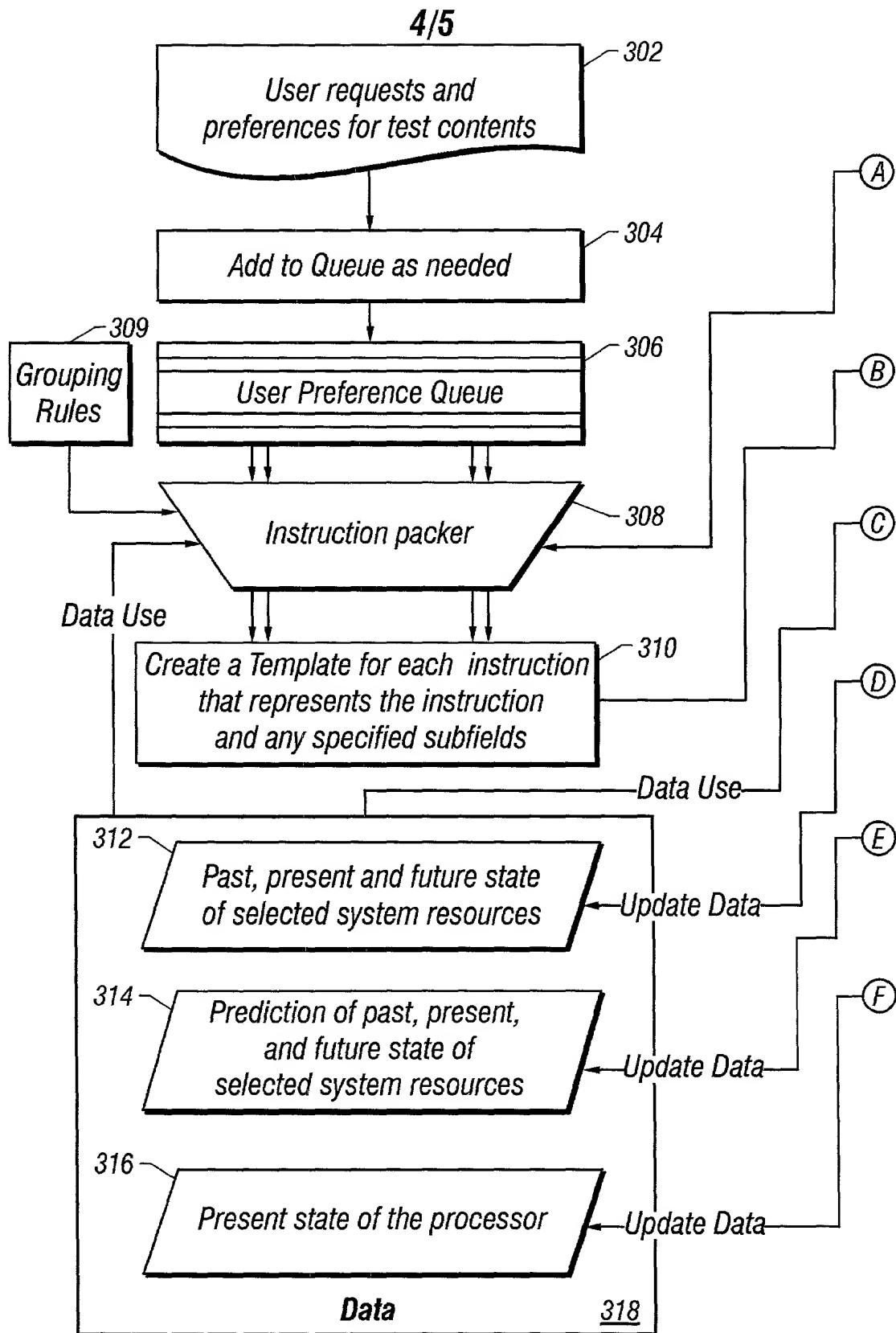


FIG. 4A

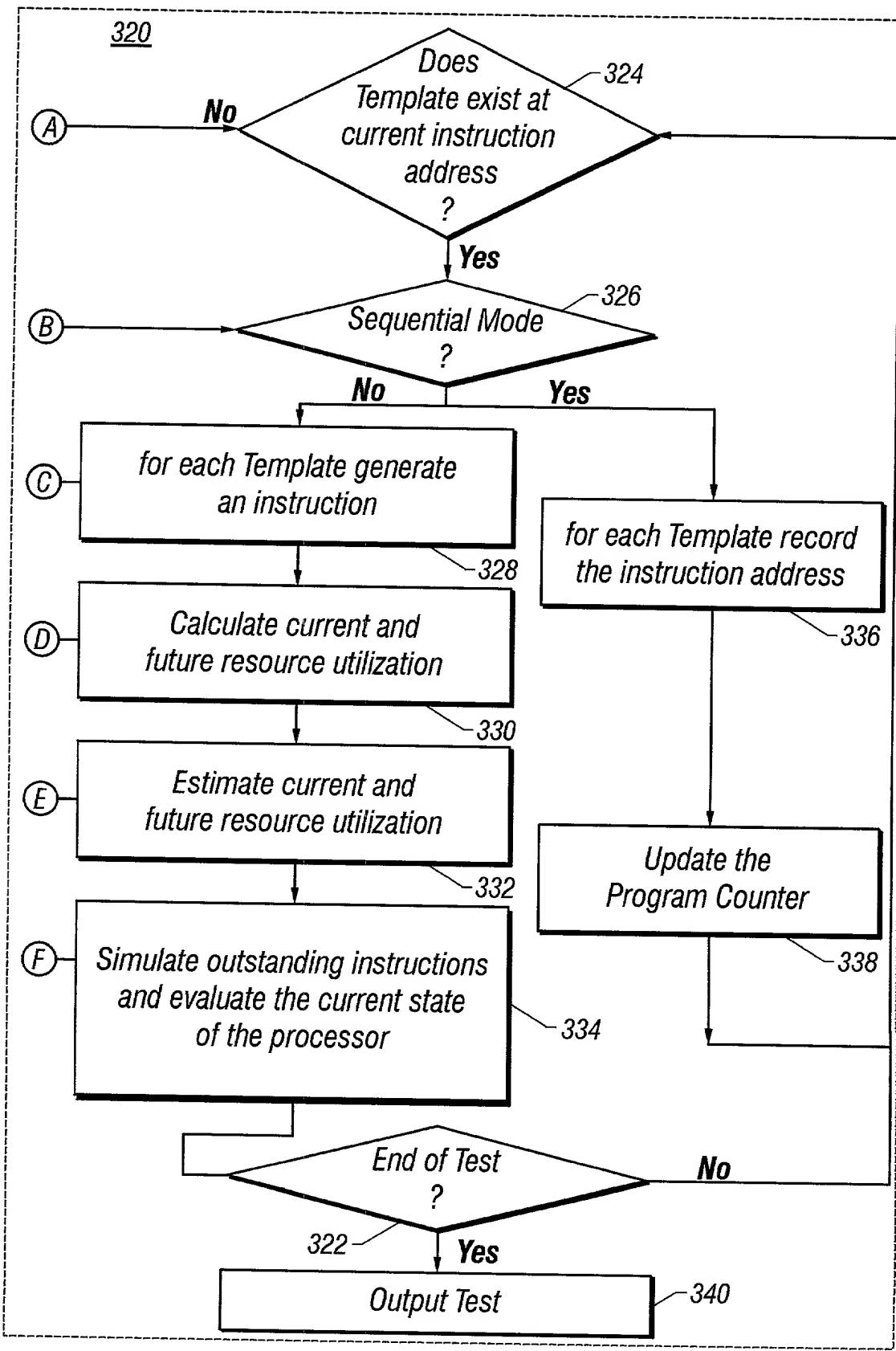


FIG. 4B

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Attorney Docket Number	62061.0105
First Named Inventor	Cavanaugh
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Method and Apparatus that Simulates the Execution of Parallel Instructions in Processor Functional Verification Testing

the specification of which

(Title of the Invention)

is attached hereto

OR

was filed on (MM/DD/YYYY) as United States Application Number or PCT International

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60/165,204	11/12/1999	<input type="checkbox"/> Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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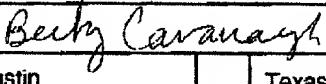
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Name of Sole or First Inventor:		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle if any)		Family Name or Surname					
Becky		Cavanaugh					
Inventor's Signature			Date	10/16/00			
Residence: City	Austin	State	Texas	Country	USA	Citizenship	US
Post Office Address	6405 Abilene Trail						
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City	Austin	State	Texas	ZIP	78749	Country	USA
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Inventor's Signature	<i>Robert Douglas Gowin</i>						Date 10/17/2000
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Post Office Address	9500 Dessau Road, No. 1214						
Post Office Address							
City	Austin	State	Texas	ZIP	78756	Country	USA
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Given Name (first and middle (if any))		Family Name or Surname					
Eric T.		Hennenhoefer					
Inventor's Signature							Date
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Post Office Address							
City	Austin	State	Texas	ZIP	78735	Country	USA
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Page 3 of 3

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Inventor's Signature						Date	
Residence: City	Austin	State	Texas	Country	USA	Citizenship	US
Post Office Address	9500 Dessau Road, No. 1214						
Post Office Address							
City	Austin	State	Texas	ZIP	78756	Country	USA
Name of Additional Joint Inventor, if any:		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])			Family Name or Surname				
Eric T.			Hennenhoefer				
Inventor's Signature	<i>Eric T. Hennenhoefer</i>					Date	10/14/00
Residence: City	Austin	State	Texas	Country	USA	Citizenship	US
Post Office Address	5748 Republic of Texas Boulevard						
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City	Austin	State	Texas	ZIP	78735	Country	USA
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U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor:	<input type="checkbox"/> A petition has been filed for this unsigned inventor						
Given Name (first and middle if any)			Family Name or Surname				
Becky			Cavanaugh				
Inventor's Signature						Date	
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Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

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DECLARATION

ADDITIONAL INVENTOR(S) Supplemental Sheet

Page 3 of 3

Name of Additional Joint Inventor, if any:		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
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Name of Additional Joint Inventor, if any:		<input type="checkbox"/> A petition has been filed for this unsigned inventor					
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Residence: City		State		Country		Citizenship	
Post Office Address							
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